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A Modified g_m Boosting Transimpedance Amplifier with Channel Length Variation for Fiber Optical Communications

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ABSTRACT

The design and simulation of a transimpedance amplifier (TIA) with different channel length is presented. The circuit consists of a Common Gate-Common Source (CG-CS) with an active feedback input stage followed by another Common Gate-Common Source stage. A series of different channel lengths (45 nm, 90 nm, 130 nm) were applied which are similar to the channel length modulation for a single channel length topology. In this work, the main focus is on obtaining the minimum input referred noise current and power consumption. The simulation results for this circuit were obtained as follows: Input referred noise current of (20.52 $pA/\sqrt{Hz}$, 16.67 $pA/\sqrt{Hz}$, 15.19 $pA/\sqrt{Hz}$) with a power consumption of (0.803 mW, 379.0 mW, 227.0 mW) corresponds to the above channel length series with a TIA gain of (44.02 dBΩ, 43.00 dBΩ, 44.08 dBΩ) at a bandwidth of (1.58 GHz, 1.56 GHz, 1.30 GHz) on series with a constant supply voltage of 1V applied. The main motivation for above innovated results was to prove that the channel length variation behavior resembles the case of channel length modulation for a single channel length topology. Simulated results were achieved using LTspice software environment.

Keywords: CG-CS, front-end amplifier, optical preamplifier, transimpedance.

INTRODUCTION

Demand for Gbps transimpedance amplifiers (TIA) for fiber optical links showed a rapid increase in recent years in which many g_m boosting regulated cascode (RGC) techniques were utilized. A 0.25 μm InP-HBT process was implemented for TIA with multiple shunt-shunt feedback network (Fukuta *et al.*, 2020). A cascaded structure is applied with an inverter that is an active feedback network in conventional RGC topology (Taghavi *et al.*, 2013). A modified RGC with a single-ended configuration was utilized in which a common-source (CS) in the conventional RGC is replaced by a common-gate stage (CG) where an inverter stage is located after the CG stage to enhance the loop gain (Parapari *et al.*, 2021). A g_m/I_D methodology for TIA design was proposed for transistor sizing to arrive at optimal specification in 130 nm CMOS technology (Elbadry *et al.*, 2020). A high G_m differential cross-coupled RGC TIA in which negative Miller capacitance and shunt active inductor compensation were exploited in 0.18 μm CMOS process (Xie *et al.*, 2016). A 0.18 μm CMOS inverter feedback RGC TIA for 3-D flash LADAR sensor was introduced (Lee *et al.*, 2018). A shunt-shunt feedback TIA with RGC as an input stage was designed using TSMC 0.18 μm CMOS technology (Parapari *et al.*, 2020). Early literature of shunt-shunt feedback TIA using 0.18 μm CMOS technology was realized (Safar and Zaki, 2013). A TIA with RGC structure at input stage followed by a level shifter and a common source (CS) structure using 90 nm BSIM4 CMOS technology was simulated (Saffari *et al.*, 2020). A 90 nm current mirror-based TIA was simulated with CG and CS configuration (Al-Kawaz and Alsheikhjader, 2020). A CG-CS input stage TIA with active inductor feedback was reported alongside a second stage current mirror with additional local active inductor feedback (Al-Berwari and Alsheikhjader, 2023).

The aim of this work is to examine the prospect of having the channel length variation behavior resembles the case of channel length modulation for a single channel length topology. In addition, the aim is to arrive at the best optimal TIA performance in terms of low input referred noise current (spectral density) and low power consumption using channel length variation.

Input stage RGC TIA:

Low-input resistance of CG topologies is always popular for designing TIAs. It is shown in Fig. (1a) that in CG structure, the input resistance can be represented as given (Soltanisarvestani *et al.*, 2020):

$$R_{in} = \frac{R_S}{1+R_S g_{m1}} \qquad \text{..... (1)}$$

Where, $\mathrm{g_{m1}}$ is the transconductance parameter of transistor $\mathrm{M_1}$ as in equation (1), the width of $\mathrm{M_1}$ plays an important role in lowering the input resistance of a CG stage. In addition, in the RGC structure shown in Fig. (1b), the transconductance of $\mathrm{M_1}$ can beraised by a factor of $(1+\mathrm{g_m R_B})$ due to existence of transistor $\mathrm{M_2}$ as the booster amplifier stage. The input resistance of the RGC circuit can be written as in the following representation where channel length modulation is neglected for simplicity:

$$R_{in} = \frac{R_S}{1+R_S g_{m1}(1+g_{m2}R_B)} \qquad \text{..... (2)}$$

The input resistance can be reduced, if the booster amplifier gain $\mathrm{g_m R_B}$ is increased. By adding a cascode transistor, it is possible to further isolate the input capacitance in order to have a high-speed TIA. The RGC structure cannot provide sufficient gain at low supply voltage (Atef and Zimmermann, 2013), hence, a gain stage can be added which consume a low power due to the use of an active inductor for instance as its load.

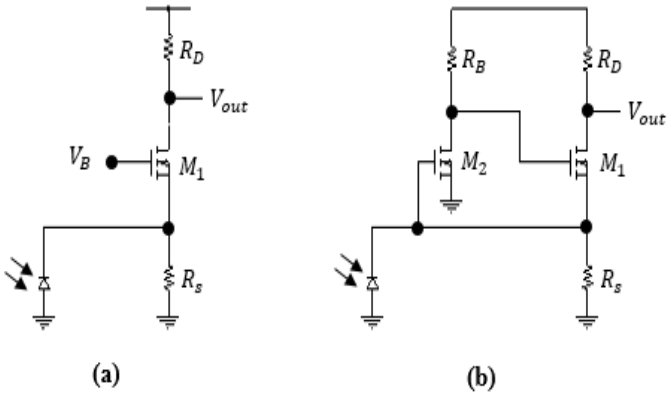


Fig. 1: (a) CG TIA topology. (b) Conventional RGC TIA topolog

MATERIALS AND METHODS

Proposed TIA topology

In Fig. (2), a two stage CG-CS TIA topology is proposed. The input stage is in shunt-shunt feedback configuration via PMOS transistor M_4 as active feedback. Following on signal path, the signal faces an input resistance $(1/g_{m1})$ at the source of transistor M_1 that is at node $in1$ in parallel with the gate resistance at node U (near infinite resistance) and the output resistance r_{O7} of the PMOS transistor M_7. Transistor M_8 acts as a pass transistor that raises the dc voltage level of node $in2$ (second CG-CS stage input) that accumulates enough voltage headroom for transistor M_{10} to conduct in CS configuration. Similarly, transistor M_2 works as a g_{m2} boosting amplifier exactly as in the case to g_{m10}. Additional transconductance parameters such as $g_{m1}$and g_{m9} are also boosted since they operate in dual configurations involving CG and CS synchronized mechanism. Having configured the input stage to work as a current gain provider followed by a CG pass transistor M_8 that raises dc voltage level at its output in conjunction with high voltage swing, then it is valid to assume that the subsequent CG-CS stage can work as a transimpedance amplifier. The active feedback via transistor M_4 is chosen since it lowers input impedance and thus pushes the input pole magnitude even further. It also allows the input stage amplifier to accommodate the photodiode capacitance ($100\ fF$) which yields a better drive capability.

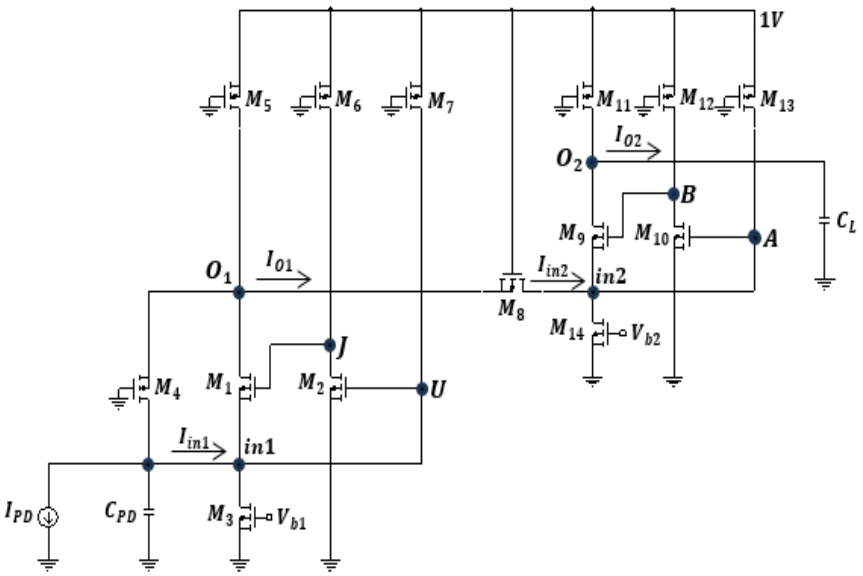


Fig. 2: Proposed TIA structure.

The small signal equivalent circuit for the input stage is demonstrated in Fig. (3). The negative feedback through the feedback admittance Y_f senses a voltage at the output node O_1 and returns a proportional current at the input node $in1$. Important to mention that Y_f controls the amount of charge through the source side of the parasitic capacitance C_{gs1}, hence controlling voltage drop across it, therefore, it could be enabling further voltage headroom for transistor M_1 to have its g_{m1} being boosted. A near virtual ground situation arises across the total input parasitic capacitance $C_{in1,tot}$ as the voltage difference between nodes $in1$ and U approaches zero. It will therefore be a very limited transfer of impedance between the two nodes with no actual voltage gain involved. The previously mentioned g_{m1} boosting impacts the drain current flow through the output node O_1 via the voltage difference between nodes J and $in1$.

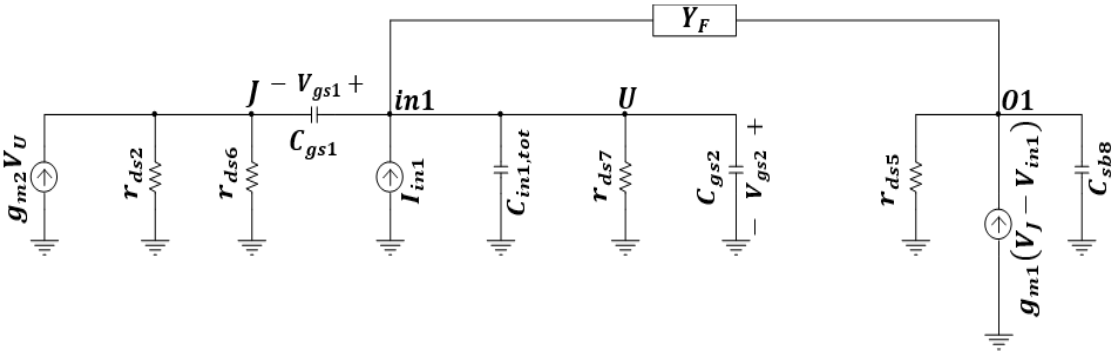


Fig. 3: Small signal model (ac equivalent circuit) of the CG-CS input stage with active feedback.

Based upon the above small signal model and following KCL nodal analysis, there no actual voltage gains from node $in1$ to node U, however, for the sake of representation, the following formula is improvised:

$$A_{in1U} = \frac{V_U}{V_{in1}} = \frac{sC_{g2}}{\left(g_{ds7}+s(C_{d7}+C_{g2})\right)} \quad \text{..... (3)}$$

The voltage gains from node U to node J is given as:

$$A_{UJ} = \frac{V_J}{V_U} = \frac{g_{m2}}{g_{ds6}+g_{ds2}+s(C_{d2}+C_{g1}+C_{d6})} \quad \text{..... (4)}$$

Whereas the voltage gains from node $in1$ to node b becomes:

$$A_{in1J} = \frac{V_J}{V_{in1}} = A_{in1U} \cdot A_{UJ} \quad \text{..... (5)}$$

The voltage gain of the input stage with active feedback is represented as:

$$A_{v1} = \frac{V_{O1}}{V_{in1}} = \frac{g_{m1}[1+|A_{in1U} \cdot A_{UJ}|]+g_{mb1}+g_{ds1}+Y_f}{g_{ds5}+g_{ds1}+s(C_{d1}+C_{d5})} \quad \text{..... (6)}$$

Where Y_f is the feedback admittance approximated by $1/r_{O4}$. The input impedance is worked out as:

$$Z_{in1} = \frac{1}{P+sC_{eq1}} \quad \text{..... (7)}$$

Where $P = g_{m1}(1 - A_{in1J}) + g_{ds1}(1 - A_{v1}) + g_{mb1} + Y_f + g_{ds3}$ and $C_{eq1} = C_{in1,tot} + A_{v1}C_{ds1}$. The f_{-3dB} bandwidth is therefore given as:

$$f_{-3dB} = \frac{1}{2\pi}\frac{P}{C_{eq1}} \quad \text{…..…… (8)}$$

$$Z_{TIA1} = A_{v1}Z_{in1} \quad \text{…..…… (9)}$$

While the output impedance of the input stage becomes:

$$Z_{O1} = \frac{r_{ds5}}{1+r_{ds5}(Y_f+sC_{sb8})} \quad \text{…….. (10)}$$

The current gain equation of the input stage with local feedback is therefore becomes:

$$A_{i1} = \frac{I_{O1}}{I_{in1}} = A_{v1}\frac{Z_{in1}}{Z_{O1}} \quad \text{…… (11)}$$

Following on similar procedure to that of the above analysis regarding the input stage with local feedback, the subsequent CG-CS stage (without feedback admittance) is a transimpedance gain provider which can have a voltage gain from node $in2$ to node A as given below:

$$A_{in2A} = \frac{V_A}{V_{in2}} = \frac{sC_{g10}}{g_{ds13}+s(C_{d13}+C_{g10})} \quad \text{…… (12)}$$

The voltage gains from node A to node B becomes:

$$A_{AB} = \frac{V_B}{V_A} = \frac{g_{m10}}{g_{ds12}+g_{ds10}+s(C_{d10}+C_{g9}+C_{d12})} \quad \text{…… (13)}$$

As the voltage gain from node $in2$ to node B is expressed as:

$$A_{in2B} = \frac{V_B}{V_{in2}} = A_{in2A}.A_{AB} \quad \text{…… (14)}$$

As a result of the above formulation, the voltage gain of the subsequent CG-CS gain is given as:

$$A_{v2} = \frac{g_{m9}(1+A_{in2A}.A_{AB})+g_{mb9}+g_{ds9}}{g_{ds11}+g_{ds9}+s(C_{d9}+C_{d11})} \quad \text{…… (15)}$$

The input impedance for this stage is shown as:

$$Z_{in2} = \frac{1}{Q+sC_{eq2}} \quad \text{…….…… (16)}$$

As $Q = g_{m9}(1 - A_{in2B}) + g_{ds9}(1 - A_{v2})$ and $C_{eq2} = C_{in2,tot} + A_{v2}C_{ds9}$. Hence, the TIA gain for this stage is illustrated as:

$$Z_{TIA2} = \frac{V_{O2}}{I_{in1}} = A_{v2}Z_{in2} \quad \text{…….…..... (17)}$$

From above derivations, and given that $I_{O1} = I_{in2}$ the overall TIA gain for the proposed circuit is represented as:

$$Z_{TIA} = \frac{V_{O2}}{I_{in1}} = A_{i1}.Z_{TIA2} \quad \text{…… (18)}$$

Noise analysis

Within CMOS transistors, operating in the frequencies of interest as in this work, there is a potential fluctuation in a random pattern inside the channel and that causes a form of channel noise. Through gate-oxide capacitance, the channel noise is permitted to the gate terminal resulting in gate

noise being induced (Kromer *et al.*, 2004). The Van der Zeil model suggests the following formulas regarding the mean square drain current noise and the mean square induced gate-noise contribution respectively (Van der Ziel and Chenette, 1978).

$$\overline{I_d^2} = 4kT\alpha g_m \quad \text{..... (19)}$$

$$\overline{I_g^2} = 4kT\delta g_g \quad \text{..... (20)}$$

As $\alpha = \gamma\, g_{d0}/g_m$, where γ is the channel thermal noise coefficient while δ is the gate noise coefficient. The shunt conductance g_g is expressed as $(\omega C_{gs})^2/5g_{d0}$ (Youssef and Haslett, 2010). The term g_{d0} is defined as the zero-bias drain conductance. Given the fact that in a CG configuration, a signal node is formed by the transistor source terminal, therefore, there is an injection of power (channel noise) at the gate and drain terminals that are in full correlation. The mean square channel thermal noise voltage (spectral density) in the proposed work contributed by the drains of transistors M_1 and M_2 can be expressed as:

$$\overline{V_{no,d1}^2} = 4kT\alpha g_{m1}(Z_{TIA1} - Z_{O1})^2 \quad \text{.....(21)}$$

$$\overline{V_{no,d2}^2} = 4kT\alpha g_{m2}\left(Z_J A_{JO1}\right)^2 \quad \text{.....(22)}$$

As the node J output impedance is characterized as:

$$Z_J = \frac{r_{ds2}r_{ds6}}{r_{ds2}+r_{ds6}(1+s(C_{g1}+C_{d2}+C_{d6})r_{ds2})} \quad \text{.....(23)}$$

While the voltage gains from node J to node $O1$ becomes:

$$A_{JO1} = \frac{M+sN}{g_{m1}A_{v1}} \quad \text{..... (24)}$$

Where, $M = A_{v1}g_{ds5} + g_{ds1}|A_{v1} - 1| - g_{m1} - g_{mb1} - g_{ds1} - Y_f$ ..... (25)

$$N = A_{v1}(C_{d1} + C_{d5}) \quad \text{..... (26)}$$

The in-built active feedback by transistor M_1 in addition to the active feedback admittance Y_f reduces the output impedance Z_J in a significant way. The mean square induced gate noise voltage (spectral density) contributed by M_1 and M_2 is expressed as:

$$\overline{V_{no,g1}^2} = 4kT\delta\frac{(\omega C_{gs1})^2}{5g_{d01}}\left(Z_{TIA1} - Z_J A_{Jo1}\right)^2 \quad \text{..... (27)}$$

$$\overline{V_{no,g2}^2} = 4kT\delta\frac{(\omega C_{gs2})^2}{5g_{d02}}(Z_U A_{UO1})^2 \quad \text{..... (28)}$$

Where Z_U is the output impedance of node U worked out as:

$$Z_U = \frac{r_{ds7}}{1+sr_{ds7}(C_{in1,tot}+C_{gs2})} \quad \text{..... (29)}$$

As the voltage gain from node U to node $O1$ is given as:

$$A_{UO1} = \frac{A_{UJ}g_{m1}+A_{Uin1}(g_{m1}+g_{mb1}+g_{ds1}+Y_f)}{g_{ds1}+g_{ds5}+s(C_{d1}+C_{d5})} \quad \text{..... (30)}$$

The summation of the mean square of the drain and gate induced noise voltages for M_1 and M_2 can be worked out as:

$$\overline{V_{no,Mx}^2} = \overline{V_{no,dx}^2} + \overline{V_{no,gx}^2} + 2|c|\sqrt{\overline{V_{no,dx}^2}.\overline{V_{no,gx}^2}} \quad \text{…..…… (31)}$$

Where c is the cross correlation between coefficient between drain and gate noise. The noise contribution of the current source M_3 is:

$$\overline{V_{no,M3}^2} = 4kT\frac{Z_{TIA}^2}{r_{o3}} \quad \text{…… (32)}$$

In which r_{o3} is the equivalent drain to source resistance of M_3. The noise contribution of equivalent load resistance is shown as:

$$\overline{V_{no,r}^2} = 4kT\left(\frac{{z_{o1}}^2}{r_{o1}} + \frac{z_J^2}{r_{o2}}A_{JO1}^2\right) \quad \text{…….…….. (33)}$$

The output of the TIA carries the total noise summed as:

$$\overline{V_{no}^2} = \overline{V_{no,M1}^2} + \overline{V_{nm,M2}^2} + \overline{V_{no,M3}^2} + \overline{V_{no,r}^2} \quad \text{…..…….. (34)}$$

Therefore, the total input referred noise current (spectral density) is expressed as:

$$\overline{I_{in}^2} = \frac{\overline{V_{no}^2}}{Z_{TIA}^2} \quad \text{...…… (35)}$$

RESULTS

In Fig. (4), as the channel length is increased from 45 nm up towards 130 nm, the TIA gain is marginally affected while the f_{-3dB} bandwidth significantly departs to low 1.30 GHz at 130 nm scale. A TIA gain of (44.02 dBΩ, 43.00 dBΩ, 44.08 dBΩ) versus a channel length series (45 nm, 90 nm, 130 nm) is shown. It is seen that as the channel length is increased from 45 nm up to 90 nm, there is not much of a difference in f_{-3dB} bandwidth with extremely limited reduction in TIA gain from 44.02 dBΩ to 43.00 dBΩ.

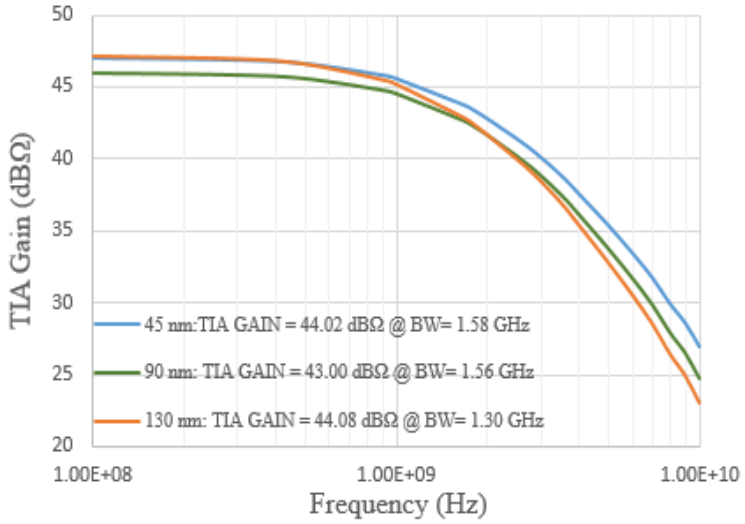


Fig. 4: Simulated TIA gain at the channel length series (45 nm, 90 nm, 130 nm) in (dBΩ).

In Fig. (5), the TIA gain in Ohm (Ω) is reported. For 45 nm scale, a 159.01 Ω is shown at a bandwidth of 1.58 GHz. The 90 nm scale simulation showed a 141.37 Ω at 1.56 GHz, while the 130 nm scale showed a160.42 Ω at 1.30 GHz.

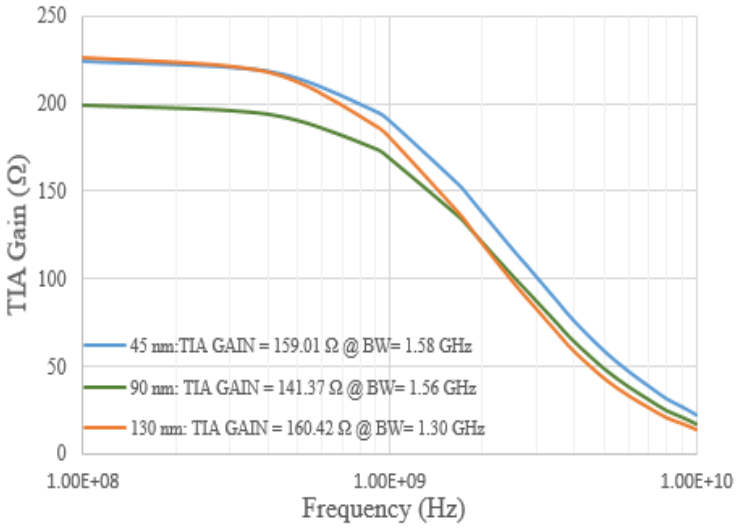


Fig. 5: TIA gain at the channel length series (45 nm, 90 nm, 130 nm) in Ohm (Ω).

In Fig. (6), the input impedance increases from 260.75Ω at 45nm scale to closer 264.66Ω at 90 nm then diverges to 311.49 Ω at 130 nm at the f_{-3dB} bandwidth series (1.58 GHz, 1.65 GHz, 1.30 GHz) versus the channel length series (45 nm, 90 nm, 130 nm) respectively.

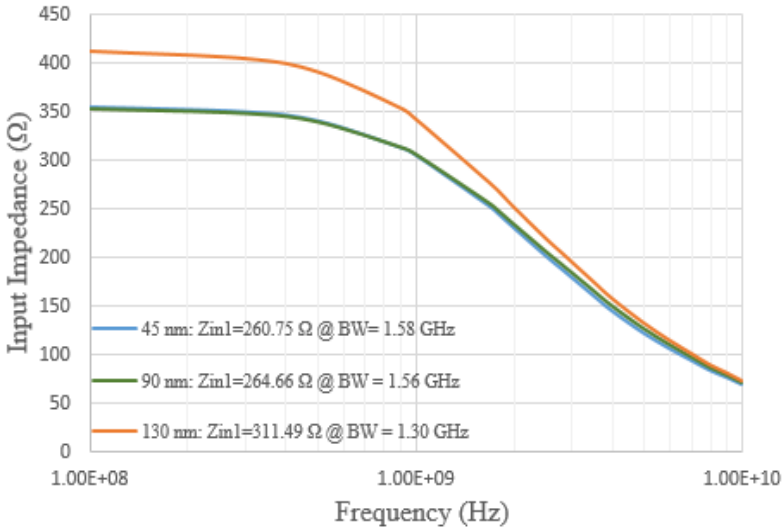


Fig. 6: Input impedance frequency response at the channel length series (45 nm, 90 nm, 130 nm).

The spectral density of the input referred noise current showed a series of (20.52 $pA/\sqrt{Hz}$, 16.67 $pA/\sqrt{Hz}$, 15.19 $pA/\sqrt{Hz}$) for the channel length series (45 nm, 90 nm, 130 nm) respectively. Interestingly, there is about 4 $pA/\sqrt{Hz}$ divergence between 45 nm and 90 nm scale versus a bandwidth change from 1.58 GHz to 1.56 GHz bandwidth difference as in Fig. (7). However, just

about 1.5 $pA/\sqrt{Hz}$ difference exists between 90 nm to 130 nm scale versus a bandwidth change from 1.56 GHz to 1.30 GHz.

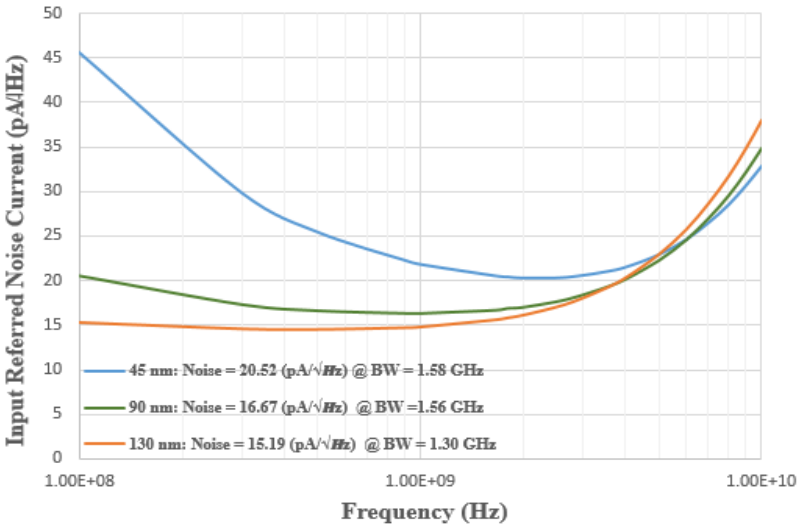


Fig. 7: Input referred noise current (spectral density) at the channel length series (45 nm, 90 nm, 130 nm).

Based on above TIA gain, input impedance, f_{-3dB} bandwidth and input referred noise current, the power consumption for the channel length series (45 nm, 90 nm, 130 nm) is reported as (0.803 mW, 0.379 mW, 0.227 mW) respectively as in Fig. (8). The same pattern reported in input referred noise current is repeated for power consumption with about to 45 nm to 90 nm despite of limited difference in TIA gain from 44.02 dBΩ to 43.00 dBΩ. Fig. (8) also shows a specific power consumption per each transistor in addition to total power consumption.

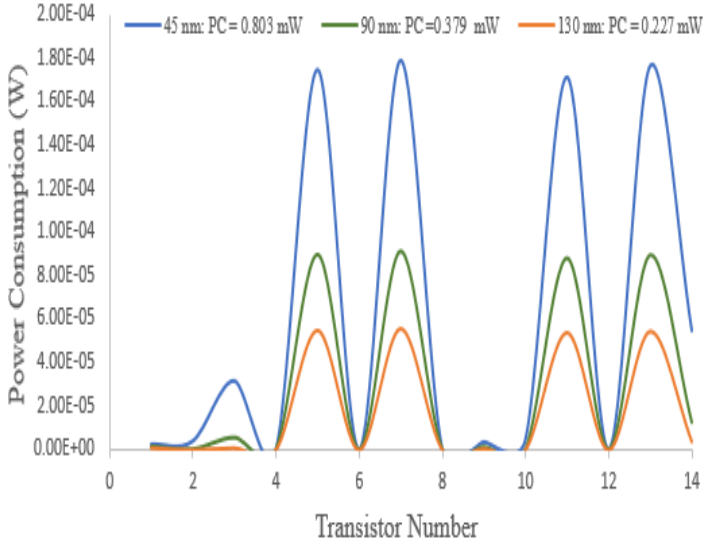
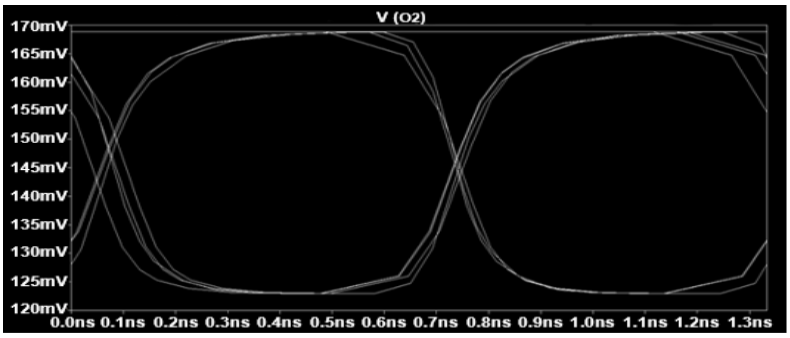


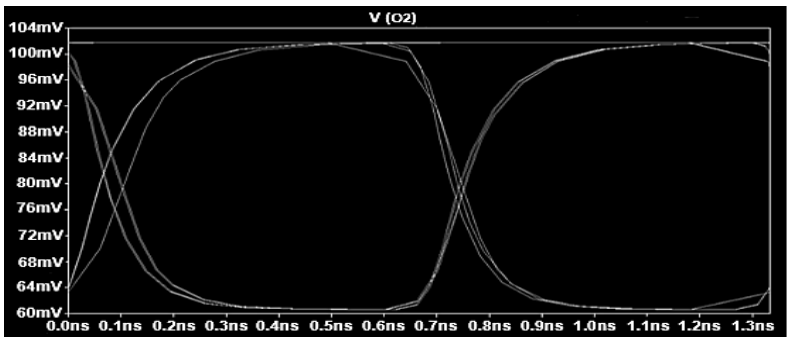
Fig. 8: Power consumption as per each transistor and total power consumption at the channel length series (45 nm, 90 nm, 139 nm).

The eye diagram for the 45 nm scale TIA topology is shown in Fig. (9a). The signal-to-noise ratio at the sampling point is 22.85 mV, while the slope that relates sensitivity to timing error corresponds to 18.72 mV versus 0.515 ns. The measure of jitter is about 0.069 ns at the time

variation of zero crossing. The decision point at the best time to sample is about 0.644 ns and that is the most open part of the eye *i.e.*, the best signal-to-noise ratio. The eye diagram for the 90 nm scale TIA topology is shown in Fig. (9b). The signal-to-noise ratio at the sampling point is 22.47 mV, while the slope that relates to sensitivity to timing error corresponds to 22.15 mV versus 0486 ns. The measure of jitter is about 0.039 ns at the time variation of zero crossing, while the decision point is about 0.629 ns. The eye diagram for the 130 nm scale TIA topology is shown in Fig. (9c). The signal-to-noise ratio at the sampling point is 24.91 mV, while the slope that relates sensitivity to timing error corresponds to 20.61 mV versus about 0.5 ns. The measure of jitter is about 0.03 ns at the time variation of zero crossing, while the decision point is about 0.641 ns. The eye diagram in Fig. (9) was simulated at 1.5 Gb/s with Pseudo-Random Bit Sequencing (PRBS) Non-Return-To-Zero (NRZ).



(a)



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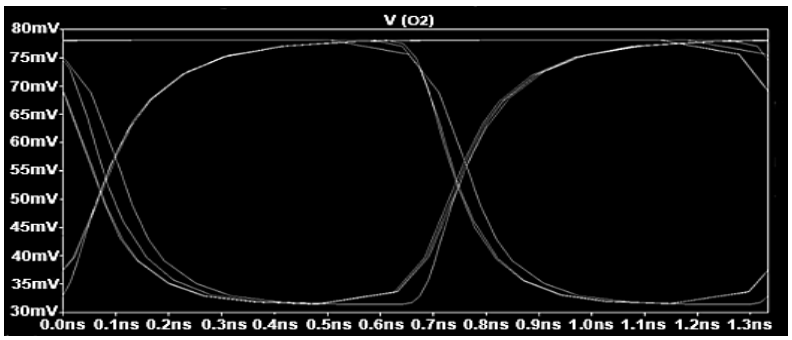

(c)

Fig. 8: Power consumption as per each transistor and total power consumption at the channel length series (45 nm, 90 nm, 139 nm).

Comparative performance analysis

In (Table 1), there can be closer results in terms of input referred noise (Kim and Buckwalter, 2012) compared to this work, while a real trade-off begins in power consumption of 9 mW versus 0.803 mW with a bandwidth of 33 GHz versus 1.58 GHz in this work, given 1V dc supply voltage with considerable diversion in TIA gain. In other literature (Xie *et al.*, 2018), a 36.6 mW power consumption can be an obstacle despite an improved TIA gain and bandwidth with low input referred noise of 12 $pA/\sqrt{Hz}$ compared to 20.52 $pA/\sqrt{Hz}$ as in this work. From channel length point of view, the 45 nm scale presents solved challenges in terms of input referred noise and power consumption (Muthukumaran and Ramachandran, 2022), however, a 10 MHz bandwidth with no specific dc supply voltage can have real draw backs on overall performance compared to this work.

Table 1: Comparative performance with other literature for 45 nm scale

Ref.	(Kim and Buckwalter, 2012)	(Xie *et al.*, 2018)	(Muthukumaran and Ramachandran, 2022)	This Work
Year	**2012**	**2018**	**2022**	**2024**
CMOS Technology	45 nm	45 nm	45 nm	45 nm
TIA Gain (dBΩ)	7.6	74.4	140	44.02
Bandwidth (GHz)	33	23	10 MHz	1.58
Input Referred Noise ($pA/\sqrt{Hz}$)	20.5	12	4.6	20.52
Power Consumption (mW)	9	36.6	0.01	0.803
dc Supply Voltage (V)	1	1	-	1

In (Table 2), the indicated 1.2 V supply voltage (Soltanisarvestani *et al.*, 2020), with improved TIA gain, bandwidth and input referred noise current falls short on power consumption performance compared to the 0.379 mW level. This work introduces the lowest power consumption compared to other literature. It can also be seen that when the 1V dc supply voltage is applied (Honarmand *et al.*, 2021), a considerable trade-off in bandwidth versus input referred noise current occurs compared to this work. From literature with no indicated dc supply voltage (Jou *et al.*, 2021), high power consumption and input referred noise constitute considerable drawback given current applications demands.

Table 2: Comparative performance with other literature for 90 nm scale

Ref.	(Soltanisarvestani *et al.*, 2020)	(Honarmand *et al.*, 2021)	(Jou *et al.*, 2021)	This Work
Year	**2020**	**2021**	**2021**	**2024**
CMOS Technology	90 nm	90 nm	90 nm	90 nm
TIA Gain (dBΩ)	50.5	41	39.8	43.00
Bandwidth (GHz)	7.3	6.5	24.8	1.56
Input Referred Noise ($pA/\sqrt{Hz}$)	13.7	33.4	50	16.67
Power Consumption (mW)	1	1.67	11.6	0.379
DC Supply Voltage (V)	1.2	1	-	1

In (Table 3), the power consumption barrier from 0.872 mW at 1.5 V (Elbadry *et al.*, 2020) to 0.227 mW at 1V as in this work still holds as it was back in (Table 2) given the indicated DC supply voltages. Drawing performance comparison with 300 mW with no specific DC supply voltage (Zhang *et al.*, 2019) is outside the scope of this work since it is focused on power

consumption reduction. The reported 3.3 V dc supply voltage (Inac *et al.*, 2021) in comparative performance also falls short of the power consumption reduction demand with 142 mW level.

Table 3: Comparative performance with other literature for 130 nm scale

Ref.	(Elbadry *et al.*, 2020)	(Zhang *et al.*, 2019)	(Inac *et al.*, 2021)	This Work
Year	**2020**	**2019**	**2021**	**2024**
CMOS Technology	130 nm	130 nm	130 nm	130 nm
TIA Gain (dBΩ)	59.885	71	66	44.08
Bandwidth (GHz)	6.9	31	40	1.30
Input Referred Noise ($pA/\sqrt{Hz}$)	7.925	14.5	9.4	15.19
Power Consumption (mW)	0.872	300	142	0.227
DC Supply Voltage (V)	1.5	-	3.3	1

DISCUSSION

In the input stage, transistor M_1 is enabled in the dual-purpose procedure. On one hand, it works as a CG amplifier that can be envisaged as a voltage amplifier with unity current gain. It receives low current at the input node $in1$ and can have relatively small Norton equivalent resistance which is replicated at the output terminal. The high output impedance of the output port in this case makes M_1 a good current source. On the other hand, when M_1 receives a signal at its gate *via* node J, it enables CS configuration with near zero input current leading to an infinite current gain and so as M_2. Since having an infinite gate resistance, M_2 phase-inverted voltage gain at the drain node J is reverted back at node $O1$ (M_1 drain) resulting in time-shift voltage swing with signal voltage at node U. Hence, there is a difference in group delay variation between the signal emanating from node $in1$ to node $O1$ compared to the signal input of node U amplified at node J and $O1$ subsequently. The active shunt feedback by PMOS M_4 accumulates fractional feedback current through its Y_f admittance. The basic function of lowering input impedance through active feedback holds true since node $in1$ resistance is in parallel with $(1/g_{m1})$ in addition to the drain resistance of M_3 as well as the infinite gate resistance of M_2 given that photodiode capacitive impedance (parasitic) is $(1/sC_{PD})$. Lower input impedance pushes towards higher absorption of photodiode current in addition to widening input pole magnitude. The r_{O4} active feedback resistor does not have a direct impact on M_1 voltage headroom as it needs not to carry a major bias current.

The subsequent combinational CG-CS stage was configured to be a TIA gain provider as mentioned earlier in which its voltage gains A_{v2} and input impedance Z_{in2} govern the drive capability of this stage. As in equation (15), the voltage gain is extended by $(1 + A_{in2A}.A_{AB})$ in which g_{m9} it is boosted considerably. The gain A_{AB} from node A to node B does compensate the absence in gain A_{in2A} considerably. However, this rise in voltage gain corresponds to lowering input impedance envisaged in equation (16).

Following Fig. (4) and Fig. (5), the TIA gain goes through several flipping patterns due to channel length variation which is a representation of channel length modulation (CLM) in "slower pace" in addition to Drain-Induced Barrier Lowering (DIBL) at 45 nm, 90 nm and 130 nm scale. With regard to channel length variation, going down from 130 nm towards 45 nm scale, the velocity saturation (near the drain) of transistors M_1, M_2, M_9 and M_{10} is extended toward the source leading to reduction in effective channel length and that subsequently causes the drain current to increase in a nonlinear manner as $V_{ds} > V_{dsat}$. The DIBL is more dominant as V_{ds} is applied to the drains of

M_1, M_2, M_9 and M_{10} in which the barrier height is lowered between drain-to-source according to previous literature (Huang *et al.*, 1992). Therefore, the threshold voltage V_{th} is reduced leading to an increase in drain current. Threshold voltage reduction is due to DIBL which is given by $-\theta(L)V_{ds}$. $\theta(L)$ as the DIBL coefficient and that is clearly depends on channel length L as follows (Liu *et al.*, 1993):

$$\theta(L) = exp(-L/2l_l) + 2exp(-L/l_l) \qquad \text{…….. (36)}$$

Considering that $l_l = \sqrt{3T_{OX}X_{dep}/\eta}$, in which X_{dep} is depletion width at the source and X_{dep}/η is the average depletion width along the channel. As a result, the early voltage at DIBL mechanism dependence on θ as a function of L becomes clear as follows:

$$V_{ADIBL} = \left(E_{sat}L + V_{gsl}\right)/\theta(L)\left(1 + 2E_{sat}L/V_{gsl}\right) \qquad \text{…….. (37)}$$

Where E_{sat} is the field magnitude at saturation region while V_{gsl} is the overdrive voltage $\left(V_{gs} - V_{th}\right)$.

From the above argument, it can be deduced that a minor fluctuation in TIA gain from 45 nm, 90 nm towards 130 nm scale as in Fig. (4) as well as in Fig. (5) is due to very limited variation in average depletion width along the channel causing the exponential function of $\theta(L)$ to have minimal effect on V_{ADIBL}. However, this minimal effect leads to the output resistances of channels (45 nm, 90 nm, 130 nm) nonlinearly changing as the mechanism is transformed from CLM-like pattern onto DIBL region. In addition to output resistance change, the threshold voltage reduction also contributes to drain current increase as mentioned before and therefore does have an impact on transconductance parameter g_m for each of the amplifying transistors M_1, M_2, M_9 and M_{10} subsequently, TIA gain is influenced. As for the channel length variation influence on f_{-3dB} bandwidth, since there is a proportional relation between the output resistance r_O with channel length L, parallel resistances r_{O1}, r_{O2}, r_{O3} and r_{O4} do represent dc input resistance R_{in1} equivalence of $(1/P)$ magnitude. Therefore, lower channel length as in 45 nm scale will lead to lower input stage resistance and ultimately expanding bandwidth.

With regard to channel length variation impact on input referred noise current, it is valid to point out that the drain current of transistor M_1 for instance is inversely proportional to channel length L within channel length series (45 nm, 90 nm, 130 nm). As a result, the transconductance parameter g_{m1} dominates equation (21) so far as the mean square of the output noise voltage at the drain of transistor M_1. In addition, the TIA gain of the input stage Z_{TIA1} within equation (21) is dominated by the voltage gain A_{v1} in a linear-like proportional relationship $A_{v1} \propto L$. However, the opposite impact of the input impedance Z_{in1} with its inverse relation to g_{m1} drives back A_{v1} impact leading to reduction in input referred noise as channel length moves up as in Fig. (7). Feedback admittance Y_f supports the opposite impact of the input impedance Z_{in1}. As for the gate side, the mean square induced gate noise voltage (spectral density) contributed by M_1 is also governed by Z_{TIA1} as in equation (27), hence it is also subject to the inverse relation between A_{v1} and Z_{in1} opposite impact given in equation (9). This concept can be extended to the gate and drain of transistor M_2 contribution on the mean square output noise voltage and subsequently input referred noise current.

As a result of above argument, the power consumption distribution as per each transistor given in Fig. (8) alongside the total power consumption (0.803 mW, 0.379 mW, 0.227 mW) for the channel length series (45 nm, 90 nm, 130 nm) respectively indicate that as channel length is moved upwards, output resistance as per each transistor is increased leading to lower drain current and hence, lower power consumption magnitude.

CONCLUSIONS

A channel length variation is examined with simulated TIA based on Common-Gate Common-Source input stage with active feedback followed by another Common-Gate Common-Source subsequent stage. It was found that a channel length variation with 45 nm, 90 nm and 130 nm scale resembles the case for single channel length topology when the proposed TIA is simulated. Furthermore, recorded low power consumption and input referred noise current (spectral density) are reported. In addition, short channel effects were overcome in which there was no clear overlap in depletion regions between drain-to-source terminals. The development of Common-Gate structure integrated with Common-Source topology enabled the alleviation of trade-off between TIA gain, bandwidth and input referred noise current spectral density. Furthermore, the reduction in power consumption to extremely lower levels is also based on above trade-off relaxation.

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تعديل g_m لتعزيز مكبر الممانعة البينية مع تغيير طول القناة لاتصالات الألياف البصرية

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الملخص

تم عرض تصميم ومحاكاة لمكبر الممانعة البينية (TIA) بطول قناة مختلف. تتكون الدائرة من بوابة مشتركة–مصدر مشترك (CG-CS) مع مرحلة دخل تغذية استرجاعية فعالة تليها مرحلة أخرى من بوابة مشتركة–مصدر مشترك. تم تطبيق سلسلة مختلفة من طول القناة (45 نانومتر، 90 نانومتر، 130 نانومتر) والتي تشبه تعديل طول القناة لطوبولوجيا طول قناة واحدة. في هذا العمل، ينصب التركيز الرئيسي على الحصول على الحد الأدنى من تيار الضوضاء المشار اليها بالدخل واستهلاك الطاقة. تم الحصول على نتائج المحاكاة لهذه الدائرة كما يلي: تيار الضوضاء المشار اليها بالدخل قدره (20.52 بيكو أمبير لكل جذر هيرتز، 16.67 بيكو أمبير لكل جذر هيرتز، 15.19 بيكو أمبير لكل جذر هيرتز) مع استهلاك طاقة قدره (0.803 ملي واط، 0.379 ملي واط، 0.227 ملي واط) يتوافق مع سلسلة طول القناة المذكورة أعلاه مع ربح TIA قدره (44.02 ديسيبل أوم، 43.00 ديسيبل أوم، 44.08 ديسيبل أوم) عند عرض نطاق ترددي يبلغ (1.58 كيكا هرتز، 1.56 كيكا هرتز، 1.30 كيكا هرتز) على التوالي مع تطبيق جهد إمداد مستمر يبلغ 1 فولط. كان الدافع الرئيسي وراء النتائج المبتكرة أعلاه هو إثبات أن سلوك تغير طول القناة يشبه حالة تعديل طول القناة لطوبولوجيا طول قناة واحدة. تم تحقيق نتائج المحاكاة باستخدام بيئة برنامج LTspice.

الكلمات الدالة: بوابة مشتركة–مصدر مشترك، مكبر النهاية–الأمامية، المكبر البصري، الممانعة البينية.